IN THE CLAIMS

1. (Currently amended) A Silicon On Insulator (SOI) structure comprising:

a silicon substrate;

a buried oxide (BOX) layer disposed on an upper surface of the silicon substrate;

a ~~SOI~~ semiconductor layer disposed on an upper surface of the BOX layer, the ~~SOI~~ semiconductor layer including an active area and a device isolation area, the device isolation area ~~including~~ of the semiconductor layer consisting of a well having a lower surface in contact with the upper surface of the BOX layer, the well including additional impurity ions compared to the active area;

a field oxide film disposed on an upper surface of the well;

a first gate line disposed over a portion of the active area and a portion of the field oxide film, the active area disposed along two sides of the first gate line;

an insulation layer disposed on an upper surface of the active area and an upper surface of the field oxide film; and

a Local Inter-Connect (LIC) disposed in contact with the insulation layer, an upper part of a second gate line, and the active area, the LIC including a conductive material.

2. (Previously presented) The SOI structure of claim 1, wherein the conductive material comprises Tungsten.

3. (Previously presented) The SOI structure of claim 1, wherein the conductive material comprises Copper.

4. (Currently amended) A semiconductor structure comprising:

a substrate;

an insulating layer disposed on the substrate;

a semiconductor layer disposed on the insulating layer;

a well disposed in a lower part of the semiconductor layer;

a field oxide layer disposed on a surface of the well;

a first active area and a second active area disposed in the semiconductor layer, the first and second active areas adjacent to the well;

a gate line disposed across the second active area and across a portion of the field oxide layer;

an insulation layer disposed on the first active area and disposed on the field oxide layer, the insulation layer in contact with a sidewall of the gate line; and

a metal fill disposed in contact with the insulation layer, in contact with an upper surface and the sidewall of the gate line, and in contact with an upper surface of the first active area.

5. (Original) The semiconductor structure of claim 4 wherein the metal fill comprises Tungsten.

6. (Original) The semiconductor structure of claim 4 wherein the metal fill comprises Copper.

7. (Currently amended) A semiconductor structure having at least two active regions and a device isolation region, the structure comprising:

a substrate;

a buried oxide (BOX) layer disposed in contact with the substrate;

a semiconductor layer disposed in contact with an upper surface of the BOX layer, the semiconductor layer thicker in the at least two active regions than in the device isolation region, the ~~semiconductor layer including a well disposed in the~~ device isolation region ~~and in contact with the BOX layer~~ of the semiconductor layer consisting of a well, the well including additional impurity ions compared to the at least two active regions;

a field oxide film that is disposed in contact with the well and that is horizontally coextensive with the well;

a first gate line crossing over one of the at least two active regions and in contact with the field oxide film;

a second gate line crossing over another one of the at least two active regions and in contact with the field oxide film;

an insulation layer disposed in contact with the field oxide film and disposed in contact with a lower portion of the first gate line; and

a conductive metal layer disposed in contact with the insulation layer, disposed in contact with an ~~upper portion of~~ an upper surface and a sidewall of the first gate line, and disposed in contact with the another one of the at least two active areas.

8. (Previously presented) The semiconductor structure of claim 7, wherein the conductive metal layer comprises a material selected from the group consisting of tungsten and copper.